AMENDMENTS TO THE CLAIMS

1. (currently amended) An automatic gain control radio frequency (RF) signal processor, comprising:

an attenuator having an input for receiving an analog RF input signal, an output for applying an attenuated output signal, and a variable gain control input;

an amplifier having an input coupled to the attenuator output and an output;

a bandpass filter having an input coupled to the amplifier output and an output;

a single analog to digital (ADC) having an input coupled to the bandpass filter output and an output for providing a digitized ADC signal;

a digital logic circuit having an input for receiving the ADC signal, a first output coupled to the variable gain control input of said attenuator, and a second output, said digital logic circuit including signal detection logic for detecting the presence of a pulse within the ADC signal, determining a peak amplitude value of the pulse, and based on the peak

amplitude value generating an attenuation value at said first output that is applied to the variable gain control input of said attenuator; and

a first in firslt out (FIFO) buffer having an input coupled to the second digital logic circuit output and an output for producing an attenuated, gain controlled, digitized output.

2. (currently amended) A processor as in claim 1, wherein the RF input signal is an intermediate frequency (IF) signal.

3. (original) A processor as in claim 1, wherein the signal detection logic comprises:

a threshold logic for detecting the presence of a pulse within the ADC signal; and

a control logic for generating said attenuation value and for controlling a flow of data into the FIFO.

4. (currently amended) A processor as in claim 3, wherein the RF input signal is an intermediate frequency (IF) signal.

5. (original) A processor as in claim 1, wherein the digital logic circuit further comprises a digital delay at said second digital logic circuit output.

6. (original) A processor as in claim 5, wherein the signal detection logic comprises:

a threshold logic for detecting the presence of a pulse within the ADC signal; and

a control logic for generating said attenuation value and for controlling a flow of data into the FIFO.

7. (original) A processor as in claim 6, wherein the RF input signal is an IF signal.

8. (original) A processor as in claim 1, wherein the signal detection logic includes storing a desired number of samples before the RF signal is detected and a desired number of samples after the RF signal is stored in the FIFO.

9. (original) A processor as in claim 1, wherein a final data sample associated with the RF signal includes a unique bit pattern recognized by the FIFO.

10. (currently amended) A method of processing an radio frequency (RF) input signal, comprising the steps of:

(a) receiving an RF signal;

(b) inputting the RF signal to an attenuator to produce an attenuator output;

(c) applying the attenuator output to an amplifier while controlling a variable gain in the attenuator to produce a controlled amplified output;

(d) passing the amplified output through a bandpass filter to produce a filtered RF output;

(e) applying the filtered RF output to an analog to digital (ADC) to produce a digitized output signal;

(f) applying the digitized output signal to a signal detection logic to determine an attenuation value and to produce a delayed output signal;

(g) repeating steps (a) - (f) for each of a plurality of ADC data samples;

(h) establishing a threshold for detecting the presence of a pulse within the plurality of ADC data samples;

(i) applying the delayed output signal to a buffer to produce a buffered signal output; and

(j) applying the attenuation value to the attenuator to establish an updated attenuation gain value.

11. (currently amended) A method as in claim 10, wherein the RF input signal is an intermediate frequency (IF) signal.

12. (original) A method as in claim 10, further comprising the step of controlling a flow of data into the buffer.

13. (original) A method as in claim 10, further comprising the step of averaging a number of data samples from the ADC to determine a moving average pulse amplitude.

14. (original) A method as in claim 13, further comprising the step of comparing the moving average pulse amplitude to a processing threshold value.

15. (original) A method as in claim 14, further comprising repeating for a number n samples the steps of averaging a number of data samples from the ADC and comparing the moving average pulse amplitude to a processing threshold value to determine whether an assigned number m of the n averages are above the processing threshold value.

16. (original) A method as in claim 15, further comprising the step of signifying the end of the pulse when an assigned number i out of j averages are below the processing threshold value.

17. (original) A method as in claim 16, wherein the moving average is computed using four data samples.

18. (original) A method as in claim 16, wherein the end of pulse is signified when i of j averages are below a noise threshold value.

19. (currently amended) An automatic gain control radio frequency (RF) signal processor, comprising:

an attenuator having an input for receiving an analog RF input signal, an output for applying an attenuated output signal, and a variable gain control input;

an amplifier having an input coupled to the attenuator output and an output;

a bandpass filter having an input coupled to the amplifier output and an output;

a single analog to digital (ADC) having an input coupled to the bandpass filter output and an output for providing a digitized ADC signal;

a first in firslt out (FIFO) buffer having an input and an output for producing an attenuated, gain control, digitized output; and

a digital logic circuit having an input for receiving the ADC signal, a first output coupled to the variable gain control input of said attenuator, and a second output coupled to the buffer input, said digital logic circuit including signal detection logic, and said signal detection logic comprising:

a threshold logic for detecting the presence of a pulse within the ADC signal; and

a control logic for determining a peak amplitude value of the pulse, and based on the peak amplitude value generating an attenuation value at said first output that is applied to the variable gain control input of said attenuator, said control logic further controlling a flow of data into the buffer.

20. (currently amended) A processor as in claim 19, wherein the RF input signal is an intermediate frequency (IF) signal.

21. (original) A processor as in claim 20, wherein the signal detection logic comprises a field programmable gate array.

22. (original) A processor as in claim 19, wherein the control logic utilizes stored peak amplitude values of one or more previously detected pulses in order to better predict the required attenuation value.

23. (currently amended) An automatic gain control radio frequency (RF) signal processor, comprising:

amplifying and gain control means for amplifying an analog RF input signal and controlling the gain of said RF input signal;

a bandpass filter having an input coupled to the amplifying and gain control means and an output;

a single analog to digital (ADC) having an input coupled to the bandpass filter output and an output for providing a digitized ADC signal;

a digital logic circuit having an input for receiving the ADC signal, a first output coupled to the variable gain control input of said attenuator, and a second output, said digital logic circuit including signal detection logic for detecting the presence of a pulse within the ADC signal, determining a peak amplitude value of the pulse, and based on the peak amplitude value generating an attenuation value at said first output that is applied to the variable gain control input of said attenuator; and

buffer means having an input coupled to the second digital logic circuit output and an output for producing an attenuated, gain controlled, digitized output.

24. (original) A processor as in claim 23, wherein the amplifying and gain control means is a variable-gain amplifier.

25. (original) A processor as in claim 23, wherein the buffer means is a memory buffer implemented in random access memory.